***Semester : 5th***

***(Regular&Back)***

***COA & CS-505***

***Branch (s) : CSE, DD M. Tech, DD*** MBA

**kiitlogo AUTUMN END SEMESTER EXAMINATION-2014**

**COMPUTER ORGANIZATION AND ARCHITECTURE**

**[ CS-505 ]**

**Full Marks: 60 Time: 3 Hours**

***Answer any six questions including question No.1 which is compulsory.***

***The figures in the margin indicate full marks.***

***Candidates are required to give their answers in their own words as far as practicable and***

***all parts of a question should be answered at one place only.***

(Instruction format: Opcode src2, src1/dest)

Q No: Contents Marks

1. Short Questions [ 2 ×10]
2. Write the basic performance equation and explain the different parameters that affects the performance of computer.
3. What is the benefit of using multiple-bus architecture compared to a single-bus architecture.
4. Consider a two level memory the average memory access time is 70 ns. Without level1 is 100ns and level1 access time is 50ns. What is the hit ratio?
5. Write the difference between write-through and write-back protocol in cache memory.
6. Difference between memory mapped I/O and I/O mapped I/O
7. Explain Memory interleaving.
8. Find the total number of memory references for the following instructions.

(i )MOV A, R1 ( ii ) ADD R1, A

1. What is the difference between static RAM and dynamic RAM.
2. Difference between page fault and cache miss.
3. What is register transfer notation. Explain with example.
4. [ 4 × 2]
5. Explain the mechanism of virtual address translation using TLB.
6. Consider a three level memory system with access times per word 20ns, 40ns, 100ns. Hit ratios are 0.7, 0.8 and 1 respectively. If the referred word is not available in level1 get the two word block from level2 to level1 and supply the desired word to the processor. If it is not available in level2 then get a 4 word block from level3 to level2 and transfer the associated block from level2 to level1. Handover the desired word to processor from level1. what is the average access time?
7. [ 4 × 2]
8. Draw the schematic diagram of the architecture of a single bus CPU, clearly showing the general purpose, Special purpose registers and the data path. Explain the function of each component.
9. What is pipeline hazard? Explain types of hazards and write the solutions for structural hazard.
10. [ 4 × 2]
11. A computer has 64 bits instruction and 8 bit address. If there are 32 3-address instruction and 248 2-address instruction then how many 1-address instruction are possible.
12. Evaluate the arithmetic expression X=(P + Q) \* (R + S) using a general register computer with its equivalent three address, two address, one address, zero address instruction format.
13. [ 4 × 2]
14. Write the micro routine for the following instruction:

ADD 50(R1),R2

1. Draw and explain 3-bus CPU organization and write the control signals to execute following instruction using same organization

ADD R1,R2,R 3

1. [ 4 × 2]
2. Explain the details architecture of Flynn's classification.
3. A cache consists of a total of 64 blocks. The main memory contains 1024 blocks, each consisting of 16 words.

( i ) What is the size of the main memory?

( ii )What is the size of the cache memory?

( iii )How many bits are there in each of the TAG, BLOCK, and WORD field in case of direct mapping?

( iv) How many bits are there in each of the TAG, and WORD field in case of associative mapping?

( v )How many bits are there in each of the TAG, SET, and WORD field in case of 2-way set-associative mapping?

1. [ 4 × 2]
2. Explain the importance of interrupt vector in I/O Processing? What is daisy chain method for handling simultaneous interrupt request.
3. Write the IEEE 754 format for representing floating point numbers in single precision and double precision format. Represent the decimal number 10.25 using the IEEE 754 single precision floating point format.
4. Write Short Notes ( Answer any Two): [ 4 × 2]
5. RISC VS CISC
6. Locality of Reference
7. Hardwired control unit
8. DMA data transfer

Paper Setter……………………..

Moderator……………………….